Analog front end for multichannel ΔΣ ADC

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Abstract— **This paper presents one solution for analog front end circuit of the multi channel ΔΣ ADC. The proposed solution is based on a sample-and-hold circuit that provides multiplexing function as well. Circuit is meant to be custom designed block which will represent analog front end of ΔΣ ADC. ADC is aimed for measurement applications of LF input signals up to 2 kHz bandwidth. The tricky part is multiplexing that should provide data from more than three inputs but with values sampled at the same instant. Practically all the values should be stored on the appropriate capacitors with as small droop as possible. However some signals will wait longer than the other for conversion. The paper explains circuit operation and proposes procedure for circuit parameter evaluation. The complete procedure has been verified by SPICE simulation.**

Keywords- ADC; ΔΣ modulation; multiplexing; modeling; sample & hold

I. INTRODUCTION

Main goal of this paper is to provide possible solutions for resolving analog multiplexing problems in ΔΣ type of ADCs with multiple inputs. It is well known that this problem arises especially when multiplexing functionality is to be integrated together with ADC itself. In power-metering applications e.g. integrated power meters (IPM) this approach practically becomes the standard [1]. In order to justify the need for such circuit some basic consideration about ΔΣ ADCs has to be discussed first. Throughout discussion concrete example of ADC will be given as well.

Thanks to CMOS technology development, more complex functions can be integrated into a silicon chip. Therefore a technique established in area of telecommunications, such as ΔΣ modulation, which provides good noise attenuation becomes more attractive for ADC implementation. Good noise attenuation implies high signal-to-noise ratio (SNR) which further requires higher ADC resolution. These concepts enable design of ADCs with resolution up to 22-24 bits. Moreover implementing with Switch Capacitor (SC) circuits afford robust designs with very high resistance to analog components mismatch. Practically, every contemporary IPM contains oversampling ΔΣ ADC with sampling frequency, f_S, that can be tens or hundreds times higher than Nyquist frequency. Basic principle behind ΔΣ ADC is shaping quantization noise with high pass (HP) transfer function, while preserving spectral content of the input signal. This is provided with so called ΔΣ HP loop filtering i.e. modulation [2]. After modulation, the converted signal is further filtered using adequate digital filter.

As claimed in [3] classic ΔΣ ADC is not preferable for multiplexing applications. It is more useful to use ΔΣ modulators with reset signal introduced. ΔΣ ADCs with this property are known as singe-shoot or incremental ADCs. In order to determine when to activate the reset signal one must determine duration of conversion for one input signal sample. Knowing this one can calculate minimal number of clock cycles at f_S rate for the loop filter. It is of crucial importance that input signal must be held as constant as possible during conversion process. Other ways minimal number of clock cycles cannot be estimated correctly. These issues are well discussed in [4] and [5]. In fact ΔΣ ADC published in [5] will represent the load for the analog front end (AFE) circuitry that is the topic of this paper. Particularly, this ADC should acquire voltages and currents of a three-phase power grid system. Therefore the project specifications are:

- three input channels
- LF bandwidth up to f_{BW} = 2048 Hz
- SNR of at least 80 dB
- Output data sublimated in form of three 16-bit wide words (for each phase of three–phase power grid)
- Output data provided to DSP at rate of f_{DSP} = 4096 Hz

More about the whole system on chip solution developed in LEDA laboratory can be found in [6].

It is important to note that all signals should be

1. sampled simultaneously and
2. converted by the same ADC.

The first requirement comes after the need to avoid the error caused by fake discrepancies in phase angles. The second appears with the goal to reduce chip area and to diminish errors due to mismatch in ADC hardware. However the conversion needs some time so that ADC require constant signals at all its inputs until the conversion of all signals completes. Obviously the analog front end necessitates implementation of Sample-and-Hold (SH) function. Besides, this block should provide multiplexing (MX) of three input signals as well.

Figure 1 depicts the conceptual idea of used ADC structure. For the sake of clarity characteristics of signals are shown at each interconnecting point between blocks in fig. 1. Dashed arrows point to appropriate signal frequency while the waveforms (below) illustrate signal's shape.

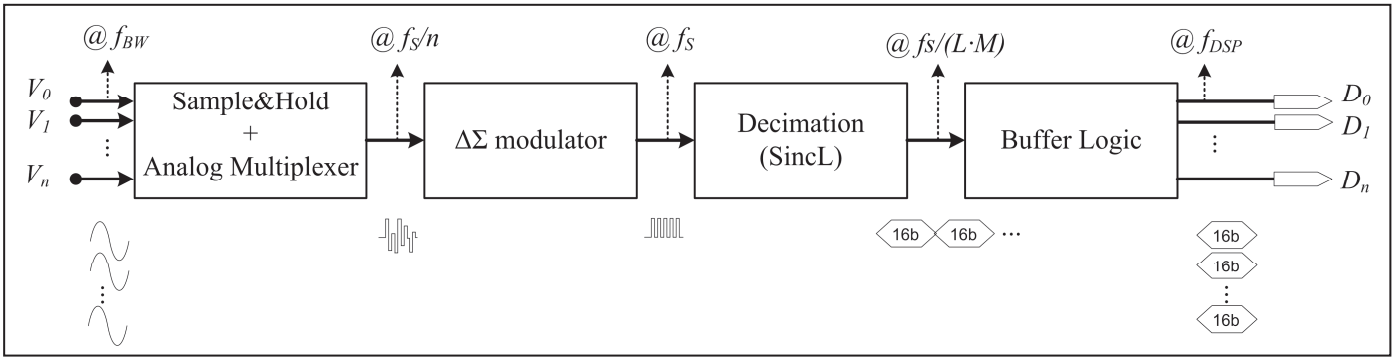


Figure 1. Generalized block diagram of multichannel ΔΣ ADC

L and *M*, denote order of the Sinc filter and oversampling ratio, respectively. V_i represents analog input while D_i represents its digital output, where $i = 0, 1 \ldots, k\text{-}1$ and *k* equals the number of channels.

Each of input analog signals should be held for n/f_S time period, where *n* is the minimal number of f_S cycles needed for obtaining 16 bit resolution [5]. During this interval sampled signal is modulated, decimated and stored in Buffer Logic block. This completes one conversion cycle. At the end of one conversion cycle modulator and decimation filter must be reset. In this way all residual values from previous signal conversion are neutralized and the next input signal can be safely processed.

After sampled values of all input signals are acquired and stored, their 16-bit digital representatives are sent in parallel towards DSP at f_{DSP} rate.

The following section describes the adopted time schedule of appropriate control signals. The third section considers the structure of proposed AFE together with a methodology for evaluation of sample capacitance value. The fourth section presents complete solution for proposed AFE with appropriate SPICE model. The subsequent section shows results of time domain simulation which verifies operation of the proposed solution. The final section summarizes the obtained results.

II. CONTROL SIGNALS TIMING

Before discussing circuit topology it is of crucial importance to establish right time schedule of control signals for both SH and MX operation. To ensure synchronization of all input signals they must be sampled at the same time. Besides, the sampling time should be the same for all signals as well. Each signal should be held for the same period. Hold period must be equal to one complete conversion cycle. Since digital part of the chip requires f_{DSP} data rate, conversion of all input signals must be performed in time window of $1/f_{DSP}$. Therefore for three input signals the following equality can be established:

$$t_{DSP} = 3t_c + t_{smpl}, \tag{1}$$

where $t_{DSP} = 1/f_{DSP}$ is DSP data rate, $t_c = n/f_S$ is required interval for conversion of one signal, and t_{smpl} is time required for sampling.

In order to provide uniformly charging/discharging of the sampling capacitor in the SC circuit, it is adopted $t_{smpl} = t_c$. From (1) one can calculate f_S as:

$$f_S = 4nf_{DSP}. \tag{2}$$

According to [4] when using Sinc3 filter and the second order ΔΣ Cascade of Integrators (CIFF) modulator, *n* is estimated to 768. For f_{DSP} = 4096Hz, oversampling frequency i.e. modulator's clock frequency is then f_S = 12582912 Hz ≈ 12.6MHz. This is adopted to be minimal clock frequency for the modulator. As stated in [3] it is wise to perform reset of the modulator and decimator for a several clocks. Since this interval is quite small comparing to whole conversion cycle time it can be included into the hold interval. As a sanity check one can easily prove this fact. For example let number of clock intervals for reset be, n_{rst} = 16. Therefore reset interval, t_{rst} will last for $n_{rst}/f_S \approx 1.27$ μs, while duration of the whole conversion cycle is $n/f_S \approx 61$ μs. It can be concluded that reset interval will be about 2% of the whole conversion cycle. Choosing n_{rst} = 4 will decrees this percentage below 1 percent. Table I summarizes reset interval percentage in conversion cycle for commonly used n_{rst}, *n*=768 and $f_S \approx 12.6$MHz

TABLE I. RESET INTERVAL PERCENTAGE IN CONVERSION CYCLE

n_{rst}	$100 \cdot t_{rst}/t_c$ [%]
16	2.08
8	1.04
4	0.52

Time schedule of appropriate signals is given in fig. 2. Sample and hold operations are marked with *S* and H_i, for i= 0, 1, 2, respectively. Case where sampling time equals to the conversion time and without space for reset interval is depicted in fig. 2.a. Fig. 2.b shows time schedule of signals with reset interval incorporated in the hold time.

In this way, f_S can stay as minimal as possible but not to deteriorate SC circuit operation.

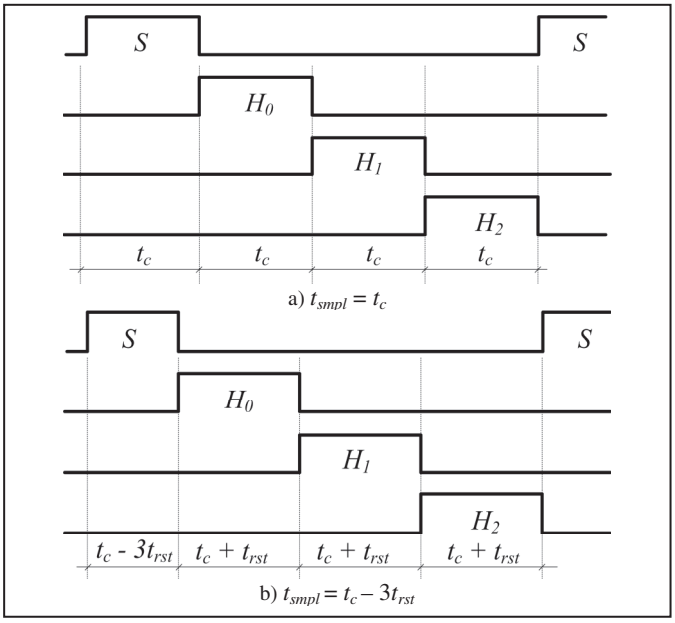


Figure 2. Time schedule of selection signals

The following section will deal with basic building block of the proposed AFE and its realization with SC circuit. The procedure for choosing capacitance value of sampling capacitor will be given as well.

III. SAMPLE AND HOLD CIRCUIT

It is already well known that SC circuits operate in two complementary, non-overlapping clock phases [7]. Fig. 3.a presents simplified version of the proposed SH circuit. Although the circuit will be realized as fully differential structure, its operation will be described on single-sided topology. This circuitry implements one capacitor, C, for both sampling and holding the charge proportional to input voltage, V_i. V_{CM} represents input and output common mode voltage, while V_{OS} represents offset voltage of operational transconductance amplifier (OTA). Proper circuit operation ensures two non-overlapping clocks denoted as Φ_1 and Φ_2. This technique is known as correlated double sampling (CDS). It requires additional controlling signal depicted as Φ_{11}. Fig. 3.b illustrates waveforms of implemented clocks. It should be noted that time axis is in $1/t_c$ units where m represents ordinal of SH cycle.

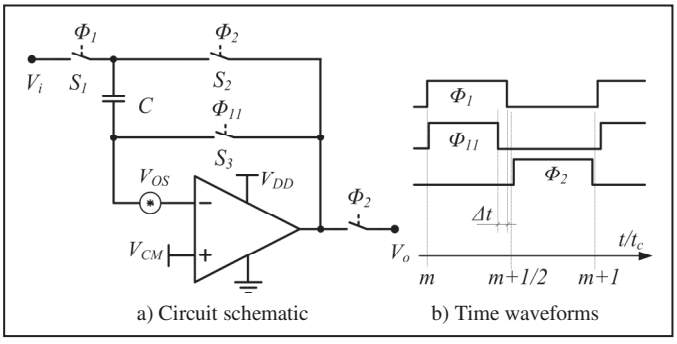


Figure 3. Simplified version of SH circuit

In fig. 3.b one can see that Φ_{11} turns off switch S_3 shortly before S_1 is turned off. For this amount of time, marked as Δt, OTA is left in open loop with high input impedance allowing V_{OS} to be accumulated on C together with the input voltage sample. Practically at the end of Φ_1 phase, when S_1 is turned off, the capacitor is charged on:

$$q_C = C(V_i[m] - V_{CM} \pm V_{OS}). \quad (3)$$

This completes the sample phase.

The hold phase begins with S_2 switching on. Now the charge on C becomes:

$$q_C = C(V_o[m+1/2] - V_{CM} \pm V_{OS}) \quad (4)$$

Since the hold phase is relatively small comparing to the period of input signal, voltage on C cannot significantly change its value. Practically $V_o[m + 1/2]$ equals $V_o[m + 1]$. Knowing this and equaling (3) and (4) one can see that V_{CM} and V_{OS} terms are canceled leaving the output voltage equal to sampled input voltage. It should be noted that output voltage is delayed by one clock cycle comparing to input voltage. Also from functional point of view clock signals Φ_1 and Φ_{11} are the same. Therefore, when confirming function of the circuit one can adopt $\Phi_1 = \Phi_{11}$, which is the case in this paper.

Now let's consider sizing of sampling capacitor in more detail. When the circuit is in intermediate state between sample and hold phases, SC structure from fig. 3.a can be modeled as depicted in fig 4. R_{off}, denotes switch off resistance; r_0 and g_m stand for output resistance and transconductance of OTA, respectively. Since node x is approximately at potential V_{CM} with assumption that input impedance is adjusted, most of the leakage current is going through the path depicted with dashed arrow in the fig. 4.a. Therefore, bearing in mind that $r_0 \ll R_{off}$, the equivalent circuitry simplifies as fig. 4.b shows.

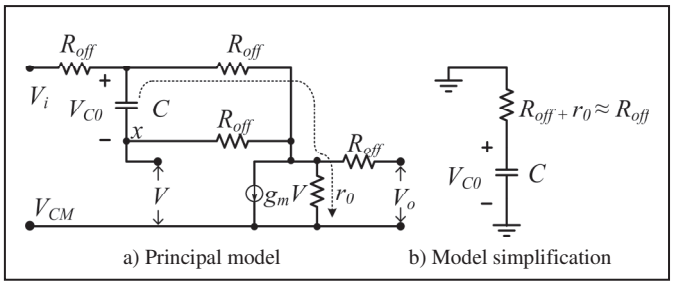


Figure 4. Model of SC circuit from Fig. 3 during intermediate interval between sample and hold phases

Assuming that the capacitor voltage at the end of the sampling phase is V_{C0}, the expecting voltage drop (according to fig. 4.b) will be:

$$V_C[t] = V_{C0} e^{-t/\tau}, \quad (5)$$

where time constant $\tau = R_{off} C$. According to fig. 2.b, worst case for the duration of the considered intermediate state is $2(t_c+t_{rst})$. The required value of C is,

$$C = \frac{2(n+n_{rst})}{f_S R_{off} \ln \frac{V_{C0}}{V_C[2(t_c+t_{rst})]}}. \quad (6)$$

In (6), $V_C[2(t_c + t_{rst})]$ is the voltage on capacitor at the end of the considered intermediate state. This voltage further can be expressed in terms of percentages of V_{C0} as:

$$V_C[2(t_c+t_{rst})] = (1-k/100)V_{C0}, \quad (7)$$

where k is the percentage of the allowed voltage drop. Finally substituting (7) into (6) gives:

$$C = \frac{2(n+n_{rst})}{f_S R_{off} \ln \frac{100}{100-k}}. \quad (8)$$

For specified R_{off}, n, f_S and acceptable percentage of capacitor voltage drop, k, one can estimate the capacitance. Fig. 5 shows capacitance v.s. voltage drop percentage for linear increase of R_{off} from 10MΩ to 100MΩ in steps of 10MΩ as a parameter.

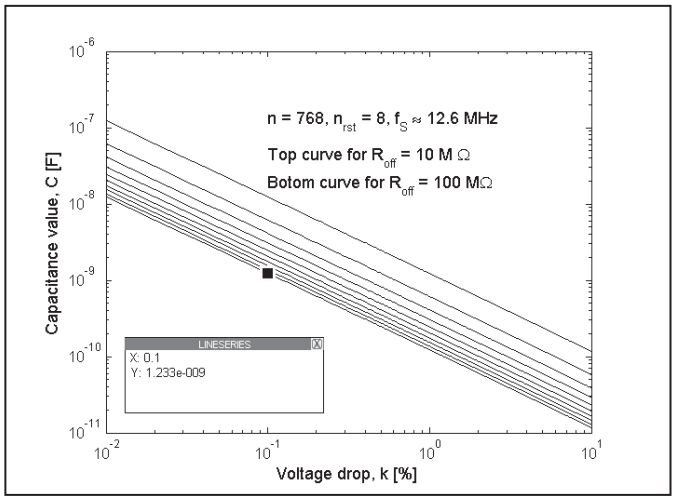


Figure 5. Dependence of Sampling/Holding capacitance on allowed percentage of voltage droop

Obviously, as expected, one can note that switches with larger R_{off} require smaller capacitance. On the other hand, for more accurate SH circuit, i.e. smaller voltage droop, the capacitance should rise up. It is evident that there is a tradeoff between accuracy, switch off resistance and capacitance value. An on-chip application requires smaller values of capacitance in order to save chip area. Therefore SH circuit design imposes special concern for switches with high leakage resistivity.

The following section will present the proposed AFE circuitry together with appropriate SPICE model development.

IV. Analog Front End Model for Multichannel ADC

Figure 6 illustrates structure of the proposed AFE for multichannel ADC. It is controlled by signals according to fig. 2.b. Sample phase (S) is the same for all input signals. During hold phases (H_i) sample of the appropriate input signal should appear at AFE output.

Three blocks marked with SH in fig. 6 represent fully differential version of the circuitry in fig. 3. Three voltages corresponding to R, S and T phase of the three-phase power grid are denoted with V_R, V_S and V_T respectively. V_M denotes output voltage.

In order to verify circuit functionality SPICE model is developed. OTA is modeled as ideal transconductance amplifier with DC gain of 80dBs and limited output signal to V_{DD}. The model includes V_{CM} as well. Classic SPICE model for switch with linear on/off resistance transfer curve is used. For on resistance 10Ω was used while for off 100 MΩ. Sampling capacitance value is estimated for the following conditions: n= 768, n_{rst}= 8, R_{off}= 100MΩ, k= 0.1% and fs= 12.6MHz. According to (6) capacitance value is evaluated to 1.233nF and 2nF capacitor is adopted. Assuming 65nm technology, where the dimensions of the smallest unity capacitor of 200.8fF are 10x10 μm, 2nF capacitor will occupy about fantastic 1 mm^2 of chip area. Although this value seems to be rather high it is used to confirm circuit functionality. On the other hand for voltage droop greater than 1 percent, capacitance decreases to tens pF, as Table II presents.

TABLE II. Capacitance values for voltage drop up to two percents

k [%]	0.1	0.2	0.5	1	2
C [pF]	1233	615	246	123	61

These values are far more convenient for integration in submicron CMOS processes. If, verification that includes complete ADC shows that the assumed voltage drop is not acceptable, higher capacitance value should be used. Therefore sampling capacitors cannot be integrated and will be mounted out of chip.

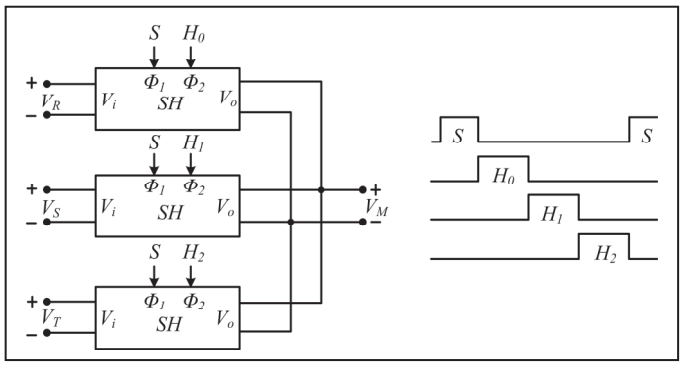


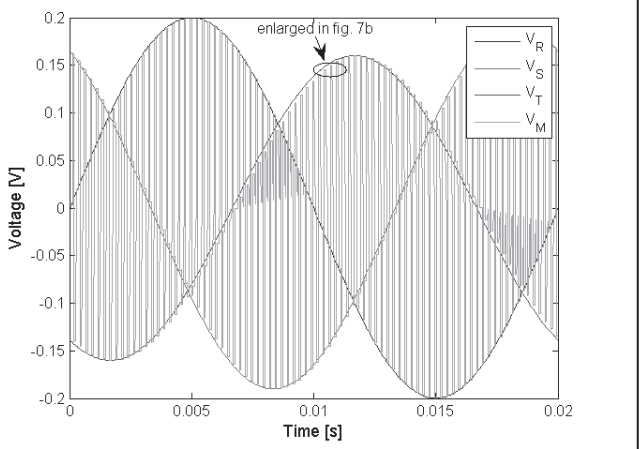
Figure 6. Blck diagram of AFE for multiplexed ADC

Results obtained for these model parameters are to be presented and commented in the following section.

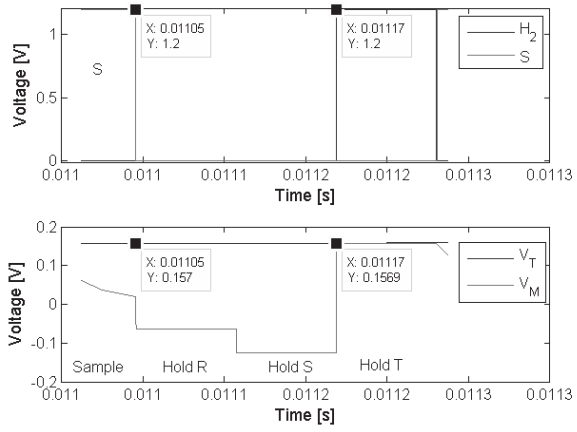
V. SIMULATION RESULTS

Fig. 7 presents results obtained after SPICE transient analysis. AFE circuit is excited with three sine-wave input signals phase shifted for 120° in order to simulate three-phase power grid. All signals are fed in differential form. Frequency of the input signals is 50Hz while amplitudes for R, S and T phase voltages are 200mVpp, 190mVpp and 160mVpp, respectively. The simulation includes V_{CM}=0.6V and V_{DD}=1.2V.

Fig. 7a shows waveforms of input and output signals for one period of input signal.



a) Time plot of input and output signals in one period of input signals, *T=20*ms



b) Details of sample and hold controlling signals (S and H_2) applied at input V_T together with the output signal V_M

Figure 7. Transient analysis results

Better insight gives fig. 7.b that illustrates detail of one complete sampling and hold cycle. This graph depicts worst case sample/hold scenario. According to fig. 6, this occurs to the last acquired signal driven by H_2. In the presented example it is V_T voltage. It waits for the longest time until acquisition. Practically the sample and hold phases for V_T are the most distant. At the end of the sample phase, i.e. in 11.05ms, the value of V_T voltage is 157mV while at the beginning of the hold phase this value drops to 156.9mV. One can easily calculate that the droop is about 0.063 percents which is even better result than 0.1 percent predicted on graph in fig. 5. Similar results are obtained for V_R and V_S voltages. One can also conclude that this result is quite expected since higher value of capacitance is adopted comparing to 1.233nF estimated with (6). Therefore for better accuracy, values higher then 2nF for capacitance should be used in this case. Extesive simultions on this level also showed two important results. First, beter then 0.05 percents for voltage drop canot be obtained even for extremely high values of capacitance. Second, values less then 50pF drastically woresn circuit operation. It should be noted that (6) is just rough estimation for capacitance value for which authors believe is good starting point in the design of the considered circuit. Thus for precise determening of capacitace value the whole sistem AFE plus ADC has to be observed and more serious modeling should be involved as well.

VI. CONCLUSION

This paper presented one original functional concept suitable to serve as analog frontend for multichannel ΔΣ ADCs. Extensive transient SPICE simulations on higher design level confirmed feasibility of the proposed solution. The obtained results exhibit satisfactory matching with theoretical behavior. Besides they exposed that the required value of sampling capacitance vary from the estimated with derived formula when tight constraints are put on capacitor voltage drop (below 0.05 percents). Therefore given formula should be carefully used. Finally one can conclude that the proposed analog frontend circuit enables simultaneous sampling and multiplexing with retained output voltage level of all input signals constant for desirable time.

ACKNOWLEDGMENT

Results described in this paper are obtained within the project TR32004 funded by Serbian Ministry of Education, Science and Technology Development

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